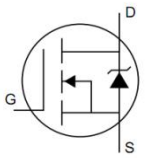
# 60V N-Channel Power MOSFET

## • General Description

It combines trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

## • Product Summary




$V_{DS}$= 60V

$R_{DS(ON)}$ = 49mΩ

$I_D$= 24A

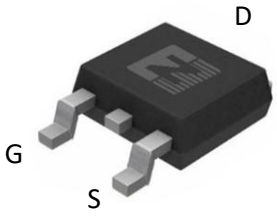
## • Features

■AEC-Q101 Qualified

■Low $R_{DS(ON)}$ to minimize conductive loss

■Low Gate Charge for fast switching

■Low Thermal resistance




TO-252

## •Application

■BLDC Motor driver

■DC-DC

■Battery protection

## •Ordering Information:

| | |
|---|---|
| Part NO. | ZMA430N06D |
| Marking | ZM430N06 |
| Packing Information | REEL TAPE |
| Basic ordering unit (pcs) | 2500 |

## •Absolute Maximum Ratings ($T_C$=25℃)

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | | 60 | V |
| Gate-Source Voltage① | $V_{GS}$ | | ±20 | V |
| Continuous Drain Current | $I_D$ | $T_C$=25℃ | 24 | A |
| | $I_D$ | $T_C$=75℃ | 19 | A |
| | $I_D$ | $T_C$=100℃ | 17 | A |
| Pulsed Drain Current | $I_{DM}$ | Pulsed; $t_p$ ≤ 10 μs; $T_{mb}$ = 25 °C; | 96 | A |
| Total Power Dissipation | $P_D$ | $T_C$=25℃ | 58 | W |
| Total Power Dissipation | $P_D$ | $T_A$=25℃ | 2.4 | W |
| Operating Junction Temperature | $T_J$ | | -55 to +175 | ℃ |
| Storage Temperature | $T_{STG}$ | | -55 to +175 | ℃ |
| Single Pulse Avalanche Energy | $E_{AS}$ | L=0.1mH, $V_{GS}$=10V, Rg=25Ω, | 13 | mJ |
| | | L=0.5mH, $V_{GS}$=10V, Rg=25Ω, | 27.3 | mJ |
| ESD Level (HBM) | CLASS 2 | | | |

## ●Thermal resistance

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Thermal resistance, junction - case | $R_{thJC}$ | | - | 2.6 | °C/W |
| Thermal resistance, junction-ambient② | $R_{thJA}$ | | - | 62 | °C/W |
| Soldering temperature | Tsold | | - | 260 | °C |

## ●Electronic Characteristics

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ =0V, $I_D$ =250uA | 60 | | | V |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ =$V_{DS}$, $I_D$ =250uA | 1.4 | 1.8 | 2.5 | V |
| Drain-Source Leakage Current | $I_{DSS}$ | $V_{GS}$=0V, $V_{DS}$= 60V | | | 1.0 | uA |
| Gate- Source Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V, $V_{DS}$ = 0V | | | 100 | nA |
| Static Drain-source On Resistance | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$= 10A | | 49 | 60 | mΩ |
| | | $V_{GS}$=4.5V, $I_D$= 8A | | 60 | 75 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ =5V, $I_{SD}$ = 10A | | 12 | | s |
| Diode Forward Voltage | $V_{FSD}$ | $V_{GS}$ =0V, $I_{SD}$ = 10A | | | 1.3 | V |

## ●Dynamic characteristics

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | Ciss | f = 1MHz, $V_{DS}$=25V | - | 715 | - | pF |
| Output capacitance | Coss | | - | 34 | - | |
| Reverse transfer capacitance | Crss | | - | 18 | - | |
| Gate Risistance | Rg | f = 1MHz | - | 1 | | Ω |
| Total gate charge | Qg | $V_{DD}$ = 15V, $I_D$ = 20A, $V_{GS}$ = 10V | - | 10.6 | - | nC |
| | Qg (4.5v) | | - | 6 | - | |
| Gate - Source charge | Qgs | | - | 2.5 | - | |
| Gate - Drain charge | Qgd | | - | 1.5 | - | |
| Turn-ON Delay time | $t_{D(on)}$ | $V_{GS}$=10V,$V_{DS}$=15V, $R_G$ =3.3Ω, $I_D$ =20A | - | 2 | - | ns |
| Turn-ON Rise time | $t_r$ | | - | 3 | - | ns |
| Turn-Off Delay time | $t_{D(off)}$ | | - | 10 | - | ns |
| Turn-Off Fall time | $t_f$ | | - | 7.5 | - | ns |
| Reverse Recovery Time | $t_{RR}$ | $V_{DD}$=20V, $dI_S/dt$ = 100A/us, $I_S$=20A | - | 29 | - | ns |
| Reverse Recovery Charge | $Q_{RR}$ | | - | 28 | - | nC |

Fig.1 Gate-Charge Characteristics

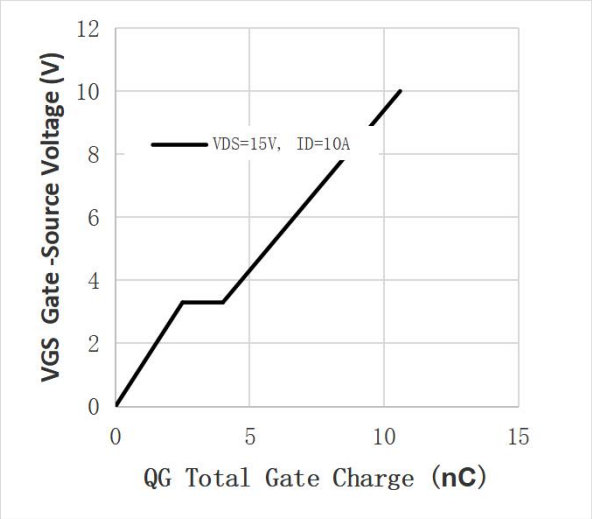



Fig.2 Capacitance Characteristics

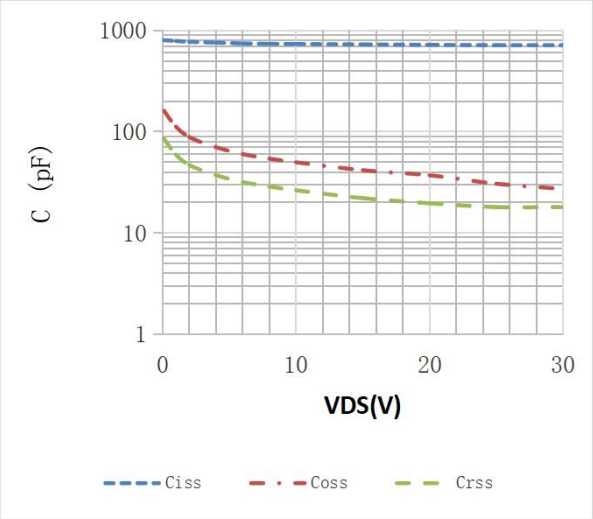



Fig.3 Power Dissipation

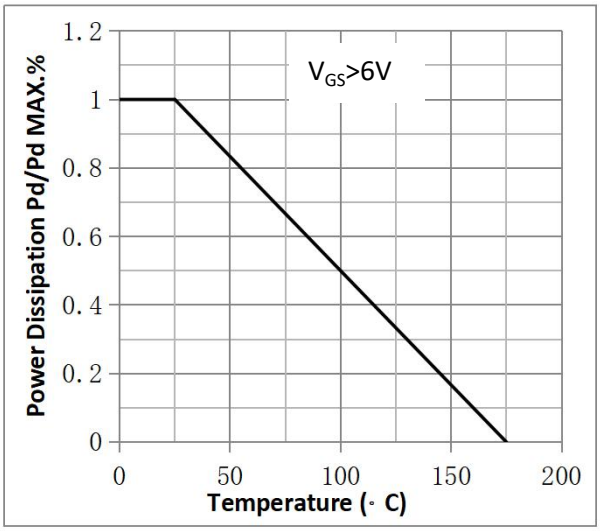



Fig.4 Typical output Characteristics

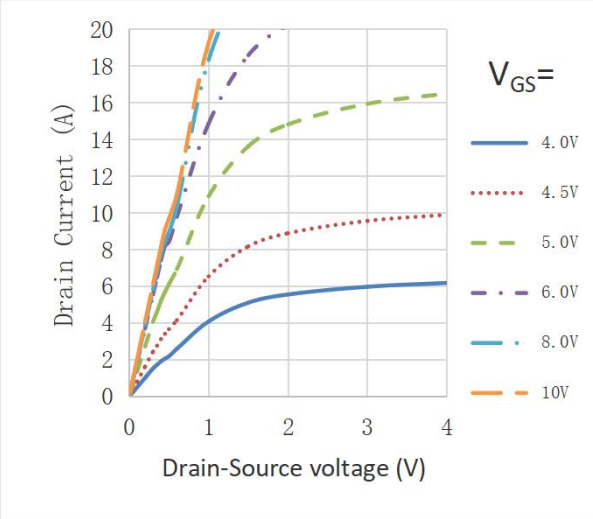



Fig.5 Threshold Voltage V.S Junction Temperature

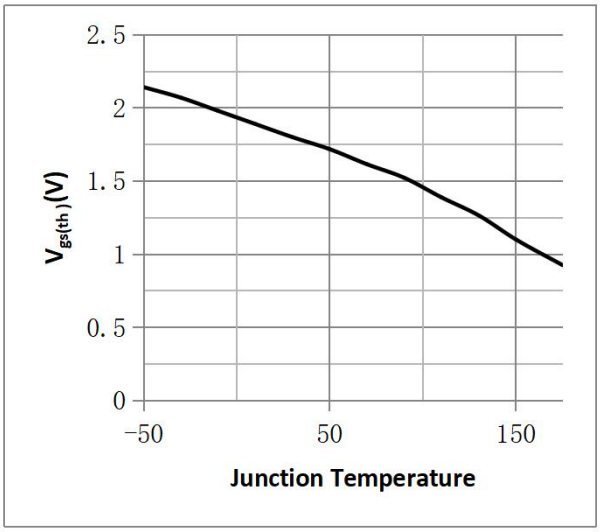



Fig.6 Resistance V.S Drain Current

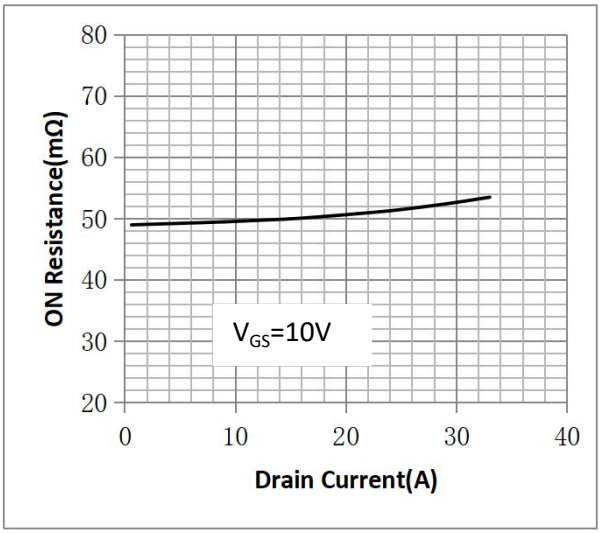


Fig.7 On-Resistance VS Gate Source Voltage

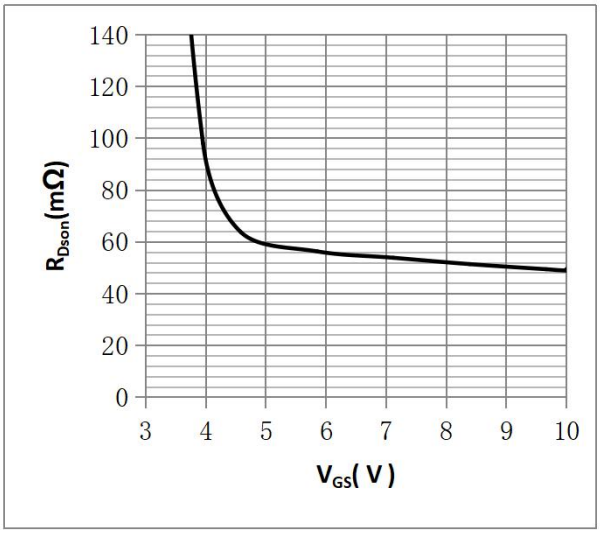



Fig.8 On-Resistance V.S Junction Temperature

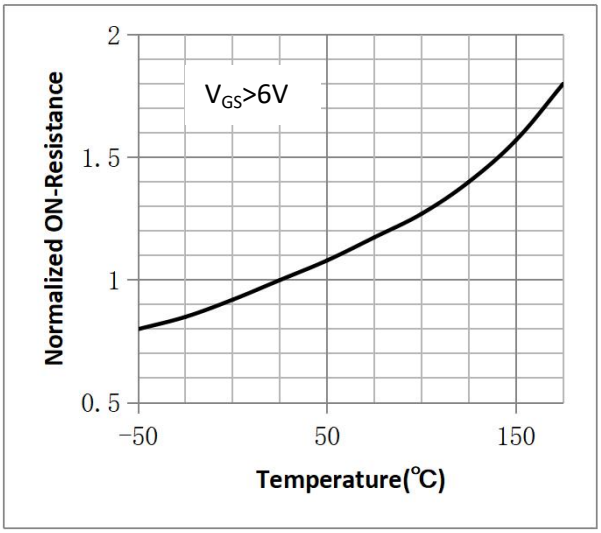



Figure 9. Diode Forward Voltage vs. Current

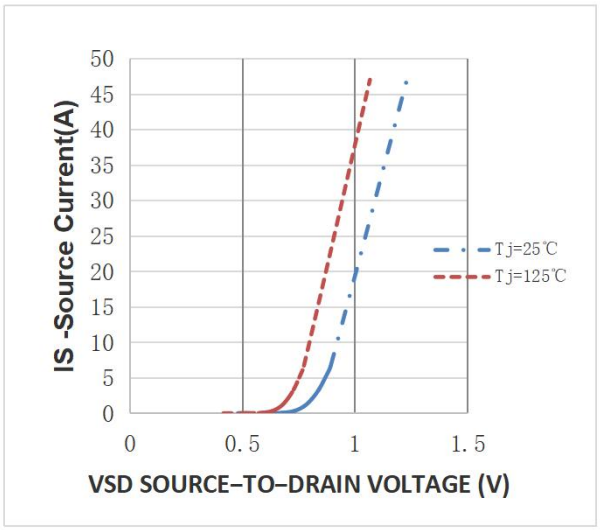



Figure 10. Transfer Characteristics

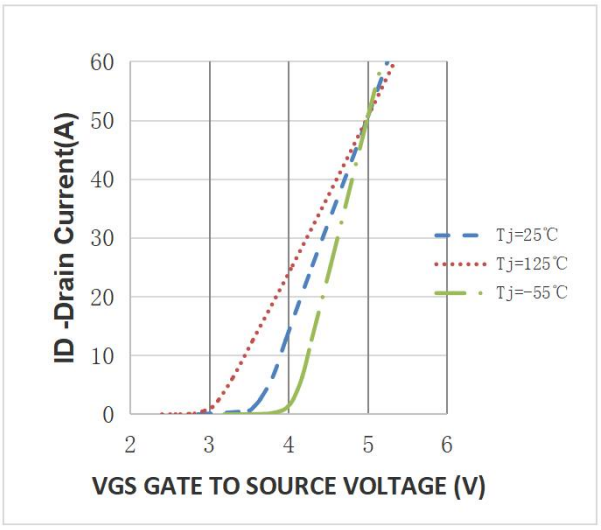



Fig.11 Safe Operating Area

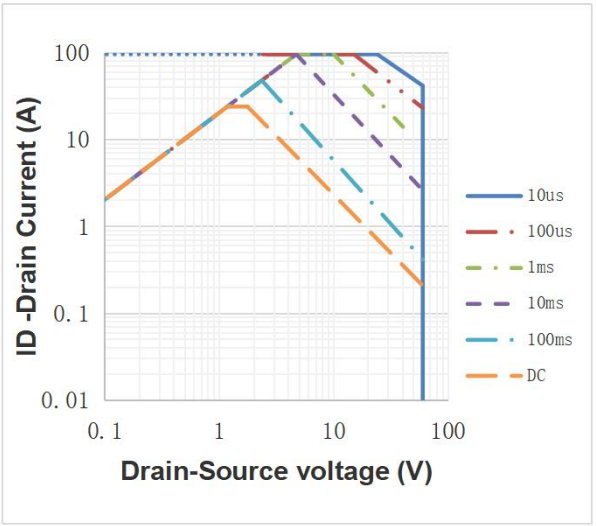
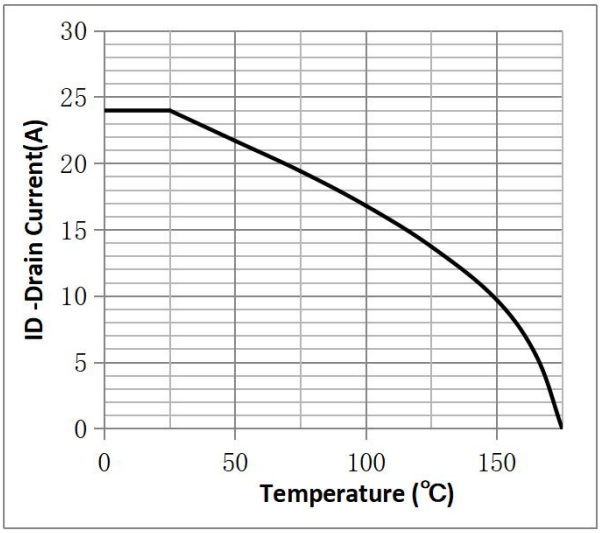
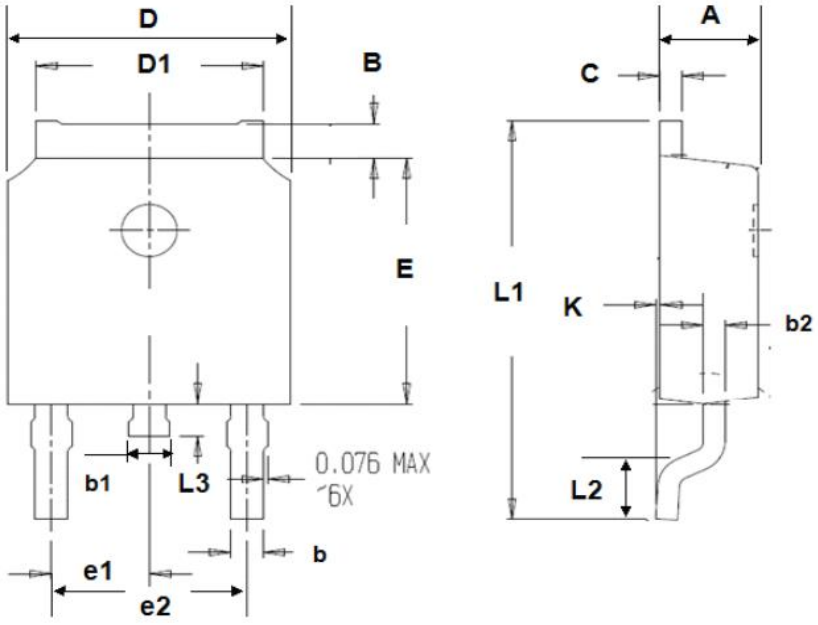



Fig.12 ID vs. Case Temperature③



## ●TO-252 Package Outline

| SYMBOL | min | max | SYMBOL | min | max |
|---|---|---|---|---|---|
| A | 2.10 | 2.50 | B | 0.85 | 1.25 |
| b | 0.50 | 0.90 | b1 | 0.50 | 0.90 |
| b2 | 0.45 | 0.70 | C | 0.45 | 0.70 |
| D | 6.30 | 6.75 | D1 | 5.10 | 5.50 |
| E | 5.30 | 6.30 | e1 | 2.24 | 2.35 |
| L1 | 9.20 | 10.60 | e2 | 4.43 | 4.75 |
| L2 | 0.90 | 1.75 | L3 | 0.60 | 1.10 |
| K | 0.00 | 0.23 | | | |



**Note:**

① Pulse : VGS=+20V/-20V, Duty cycle=50%,Tj=175℃, t=1000 hours; For DC， the following test conditions can be passed: VGS=+20V/-10V, Tj=175℃, t=1000 hours；

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate；

③Practically the current will be limited by PCB, thermal design and operating temperature. VGS=10V.

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Revision History

| Version | Date | Change |
|---|---|---|
| A | 2021.11.10 | |
| B | 2022.12.5 | 1.Add Reach,HF figure,2.ID modify |
| C | 2023.12.8 | 1.Correct Pakage Outline Dimension<br>2.Correct SOA |
| | | |
| | | |
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